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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,731	03/30/2005	Brendan P. Kelly	GB02 0239 US	1996

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EXAMINER	
WOJCIECHOWICZ, EDWARD JOSEPH	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
07/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/529,731	KELLY ET AL.	
	Examiner	Art Unit	
	Edward Wojciechowicz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As stated in the previous actions, the overall structure of the invention, and specifically the second gate, is not clearly defined. Does the inventive concept require that the second gate be formed partly within the trench? Is this a critical and necessary structural feature of the invention, or merely an optional feature that can be eliminated?

How are each of the respective source and drain regions, and each of the respective gate electrodes electrically connected to each other across all of the plurality of cells, so as to form the electrically parallel transistor cells? In addition, how many electrically parallel transistor cells are necessary to practice the invention? That is, what is the minimum number of cells needed to practice the invention?

In claim 6, the circuit configuration of the gate driver circuit is not clearly defined.

In claim 7, the overall circuit arrangement is not clearly defined. In addition, what is the structure of the low side power transistor which is connected to the high side power transistor described in claim 1? Furthermore, claim 7 describes only two transistors, a high side power transistor, and a low side power transistor. This appears inconsistent with the recitation in claim 1, from which claim 7 ultimately depends, that the claim 1 structure comprises a "plurality of electrically parallel transistor cells". How is the single low side power transistor described in claim 7 connected in series with the plurality of electrically parallel transistor cells described in claim 1? Exactly how many transistors are being described in claim 7?

In claim 8, to which of the plurality of source and drain electrodes that make up the power transistor device of claim 1 is the load connected to?

In claims 9 and 10, the overall circuit arrangement is not clearly defined as to how the components are integrated with each other.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims, 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaji (6,072,215) in view of Hu et al (2005/0269624) and Williams et al (2002/0019099). Each of the cited references teach the inventive concept of a power transistor structure which has both a vertical trench gate portion and a lateral surface gate portion to control the device.

The reference to Kawaji shows, for example in FIG. 13, a transistor structure with electrically parallel devices, having a first central trench gate (230) that enables a first vertical channel portion, and second gates (203a) and (203b) having insulated planar gate portions on a top major surface of the semiconductor body that enable lateral channel portions. Both the vertical and lateral gate portions are insulated from each other.

The reference to Hu shows a related structure, for example in 2Q, having a trench gate (40a) adjacent the body region, which enables a vertical channel, and second gate (68) is formed on the body surface and enables a lateral channel. The gates are also separated by a first insulation layer (48) that is located within and extends across the trench, with second gate material (68) thereon. Note that the second gate (68) also extends over the first gate (40a) and into the trench space formed between elements (56) on opposite sides of a trench which is "adjacent" the body region, as claimed. In addition, a second insulation layer (30) with gate material (68) thereon extends laterally both ways from the trench on the top major surface of the body, such that the second gate has an insulated trench gate portion and an insulated planar gate portion, as claimed in claim 3.

Williams et al also shows it is well known to form trench gate transistors in a closed cell geometry where the peripheral gate structures surround each transistor. See, for example, FIG. 4D.

Taken together, the cited references teach all of the claimed structural features of claims 1-4. One skilled in the art would be motivated to combine the features of Hu and Williams with the basic configuration of Kawaji in order to achieve a more compact dual gate structure, as taught by the references.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Wojciechowicz whose telephone number is 571-272-1739. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Edward Wojciechowicz/
Primary Examiner, Art Unit 2815

Edward Wojciechowicz
Primary Examiner
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EW: ew